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10/717,955 Docket No.: 08211/0200374-US0
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Letters Patent of:
Ha Chu Vu

Patent No.: 6,952,121

Issued: October 4, 2005

For: PRESCALING FOR DIVIDING FAST PULSED SIGNAL



**REQUEST FOR CERTIFICATE OF CORRECTION**
**PURSUANT TO 37 CFR 1.322**

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several errors which should be corrected.

In the Specification:

Column 2, Line 51, Delete "clock-sync" and insert -- clock_sync --.

Column 2, Line 61, Delete "clock sync" and insert -- clock_sync --.

Column 6, Line 1, Delete "counter-reset" and insert -- counter_reset --.

Column 7, Line 12, In Claim 1, after "until" insert -- after --.

Column 7, Line 63, In Claim 8, after "until" insert -- after --.

Column 8, Line 13, In Claim 9, after "until" insert -- after --.

Enclosed please find marked up copies of pages 3 & 8 of the specification. And marked up copies of pages 2, 3, & 4 of the claims.

The errors were not in the application as filed by applicant; accordingly no fee is required.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: October 27, 2005

Respectfully submitted,

By____________________

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(Also Form PTO-1050)

# UNITED STATES PATENT AND TRADEMARK OFFICE
## CERTIFICATE OF CORRECTION



PATENT NO. : 6,952,121 B1

APPLICATION NO. : 10/717,955

ISSUE DATE : October 4, 2005

INVENTOR(S) : Ha Chu Vu

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 2, Line 51, Delete “clock-sync” and insert -- clock_sync --.

Column 2, Line 61, Delete “clock sync” and insert -- clock_sync --.

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Column 7, Line 12, In Claim 1, after “until” insert -- after --.

Column 7, Line 63, In Claim 8, after “until” insert -- after --.

Column 8, Line 13, In Claim 9, after “until” insert -- after --.

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In some embodiments, a dual modulus prescaler is arranged to receive periodic input pulses. The prescaler then counts the received input pulses, and generates one prescaled pulse for every Qth input pulse. Q is a division modulus, and has a different value depending on a modulus control signal. When the prescaler generates a prescaled pulse from an input pulse, it then ignores the modulus control signal at least until the onset of a next input pulse, and sometimes until the onset of one more input pulse. A program counter generates a reset signal when the prescaler receives the Mth pulse. A swallow counter then changes the modulus control signal to a different value. Accordingly, the prescaler starts dividing by a different division integer. Even if the modulus control signal changes after the prescaler has already received the onset of the next one or two input pulses, the prescaler accounts for them properly, for dividing with the different division integer.

The invention offers the advantage that a fast pulse input signal can be used, and thus a faster clock can be generated with little additional change. There is no limitation that the period of the input pulses must be longer than how long it takes for the modulus control signal to be changed due to the reset signal.

The invention is now described in more detail.

FIGURE 1 illustrates a block diagram of some components of a circuit 100 in which the invention may be embodied. Circuit 100 generates a fast clock signal FASTOUT from a reference synchronization signal HSYNC which has a reference frequency fclkref. In addition to possibly other components, circuit 100 includes frequency/phase detector 110, which receives signal HSYNC and outputs a synchronized signal clock_sync. A fast clock generator 140 generates a fast clock signal FASTOUT from synchronized signal clock_sync. Fast clock signal FASTOUT may have a number of outputs, for example for further providing signals having different phases of a clock. A Divide-by-M counter 150 receives fast clock signal FASTOUT, and may treat it as an input pulsed signal clkin. Counter 150 also receives a counter control signal PLLDIV, which is used to select the number M by programming. Counter 150 outputs a divided down signal clkout, which includes one pulse for every M pulses of input signal clkin. Frequency/phase detector 110 compares the divided down signal clkout with signal HSYNC, to generate the synchronized clock_sync signal.

variable D0, which is one. This way, even if modulus control signal DIV4 changes (e.g. due to a very fast input clock), the operation will not be affected.

At state 830, it is inquired for the first time what is the value of DIV4. If the value is 1, then it takes two more states (840, then 810 again), for a total of N=4, to accomplish division by four. If at state 830 DIV4 is found to be 0, then it takes three more states (850, then 860, then 810 again), for a total of N+1=5, to accomplish division by five.

FIGURE 9 illustrates timing diagrams of signals resulting from a prescaler that follows the logical instructions of FIGURE 7. In addition, waveform 410 is repeated from FIGURE 6, for reference only.

A faster input clkin waveform 910 may be received, which has a period Tcf 912 shorter than period Tc 612 of waveform 410. It can be appreciated that waveform 910 is shown with the same number of pulses as the earlier clock 410, but requires less time (measured on the horizontal time axis), because it is faster, as enabled by the invention.

Pulse 914 of waveform 910 is the Mth pulse, and pulse 916 is the next pulse. Much of the behavior is similar to what is described in FIGURE 6. In other words, a prescaled pulse 924 is generated in CK45 waveform 920, in response to input pulse 914. Pulse 924, however, is generated by the instructions of FIGURE 7, and changing from state 840 to state 810 in FIGURE 8. A counter_reset pulse 634 is generated in response to prescaled pulse 924, and a change 654 is generated in response to counter_reset pulse 634. A critical path delay CPD9 962 is exhibited, which may be the same as critical path delay CPD6 662 of FIGURE 6. It should be noted that critical path delay CPD9 962 is shorter than the faster clock period Tcf 912.

FIGURE 9 illustrates concurrently this important advantage of the invention. When the prescaler receives Mth pulse 914, modulus control signal DIV 4 changes value after the prescaler has already received the onset of next input pulse 916. Thus, clocks of higher frequencies may be used. The full advantage comes from exploiting the fact that, for N=4 and the particular states of FIGURE 8, the prescaler is indifferent to modulus control signal DIV 4 for the two next input pulses, not just one. A correspondingly faster input pulse waveform can thus be used by the invention.

## AMENDMENTS TO THE CLAIMS

1. (Currently amended) A circuit for dividing periodic input pulses by a preset integer M, comprising:

a dual modulus prescaler arranged to receive periodic input pulses and to count the received input pulses for generating prescaled pulses, wherein one prescaled pulse is generated for every Qth input pulse, wherein Q is a division modulus having a value depending on a value of a modulus control signal, wherein when a prescaled pulse is generated from a selected input pulse, the modulus control signal is ignored at least until the onset of a next input pulse is received; ~~and~~

a swallow counter arranged to change the modulus control signal to a different value in response to the prescaler receiving every Mth input pulse, wherein M is a preset integer; and

a program counter to generate a reset signal in response to the prescaler receiving the Mth input pulse, and

wherein the swallow counter changes the modulus control signal in response to the reset signal.

2. (Original) The circuit of claim 1, wherein

if the ignored modulus control signal acquires a different value due to the selected input pulse, the next pulse is counted according to a correspondingly different value of Q.

3. (Original) The circuit of claim 2, wherein

when the prescaler receives a selected one of the Mth pulses, the modulus control signal changes value after the prescaler has already received the onset of a next input pulse.

4. (Original) The circuit of claim 1, wherein

the prescaler includes an OR gate for ORing the modulus control signal with another signal.

Claim 5 (canceled)

6. (Currently amended) The circuit of claim ~~5~~1, further comprising:

a frequency/phase detector arranged to receive a divided down signal generated in response to the prescaler receiving the Mth input pulse, and to output a synchronized signal in response to the divided down signal; and

a fast clock generator to generate a fast clock signal from the synchronized signal, and wherein the input pulses are derived from the fast clock signal.

7. (Currently amended) The circuit of claim ~~5~~1, wherein

the program counter is adapted to generate the reset signal in response to receiving a prescaled pulse that corresponds to the prescaler receiving the Mth input pulse.

8. (Original) The circuit of claim 7, wherein

the prescaler includes components that define state variables which are initialized to particular values when a prescaled pulse is generated, and

the state variables become initialized to the particular values also when a Power On Reset is performed.

9. (Currently amended) A device comprising:

means for receiving periodic input pulses; and

means for counting the received input pulses to generate prescaled pulses, wherein

one prescaled pulse is generated for every Qth input pulse~~,~~ wherein Q is a division modulus having a value depending on a value of a modulus control signal, and

when a prescaled pulse is generated from a selected input pulse, the modulus control signal is ignored at least until the onset of a next input pulse following the selected input pulse is received~~.~~; and

a means for generating a reset signal in response to the prescaler receiving the Mth input pulse, wherein M is a preset integer, and

wherein a swallow counter changes the modulus control signal in response to a reset signal.

10. (Currently amended) A method comprising:

receiving periodic input pulses; and

counting the received input pulses to generate prescaled pulses, wherein

one prescaled pulse is generated for every Qth input pulse, wherein Q is a division modulus having a value depending on a value of a modulus control signal, ~~and~~

when ~~a~~the prescaled pulse is generated from a selected input pulse, the modulus control signal is ignored at least until the onset of a next input pulse following the selected input pulse is received; and

generating the prescaled pulses includes:

initializing a vector of state variables when the prescaled pulse is generated, and

updating the vector during the next input pulse in a way that is indifferent to the updated modulus control signal.

11. (Original) The method of claim 10, wherein

the modulus control signal is further ignored at least until the onset of a second next input pulse following the next input pulse is received.

12. (Original) The method of claim 10, wherein

if the ignored modulus control signal acquires a different value due to the selected input pulse, the next pulse is counted according to a correspondingly different value of Q.

13. (Original) The method of claim 10, wherein

the first value of Q equals a preset number N, and

the second value of Q equals N+1.

14. (Original) The method of claim 10, wherein

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OCT 28 2005
PATENT & TRADEMARK OFFICE

Application No. (if known): 10/717,955 Attorney Docket No.: 08211/0200374-US0

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